1 Overview

The W806 chip is a secure IoT MCU chip. The chip integrates a 32-bit CPU processor with built-in UART, GPIO, SPI, SDIO, I2C, I2S, PSRAM, 7816, ADC, LCD, TouchSensor and other digital interfaces; support TEE security engine, support a variety of hardware decryption algorithm, built-in DSP, floating-point arithmetic unit and security engine, support code security permission setting, built-in 1MB Flash memory, support firmware encrypted storage, firmware signature, security debugging, security upgrade and other security measures to ensure product security features. Suitable for small appliances, smart

It can be used in a wide range of IoT fields such as home furnishing, smart toys, industrial control, and medical monitoring.

2 Pin Definition

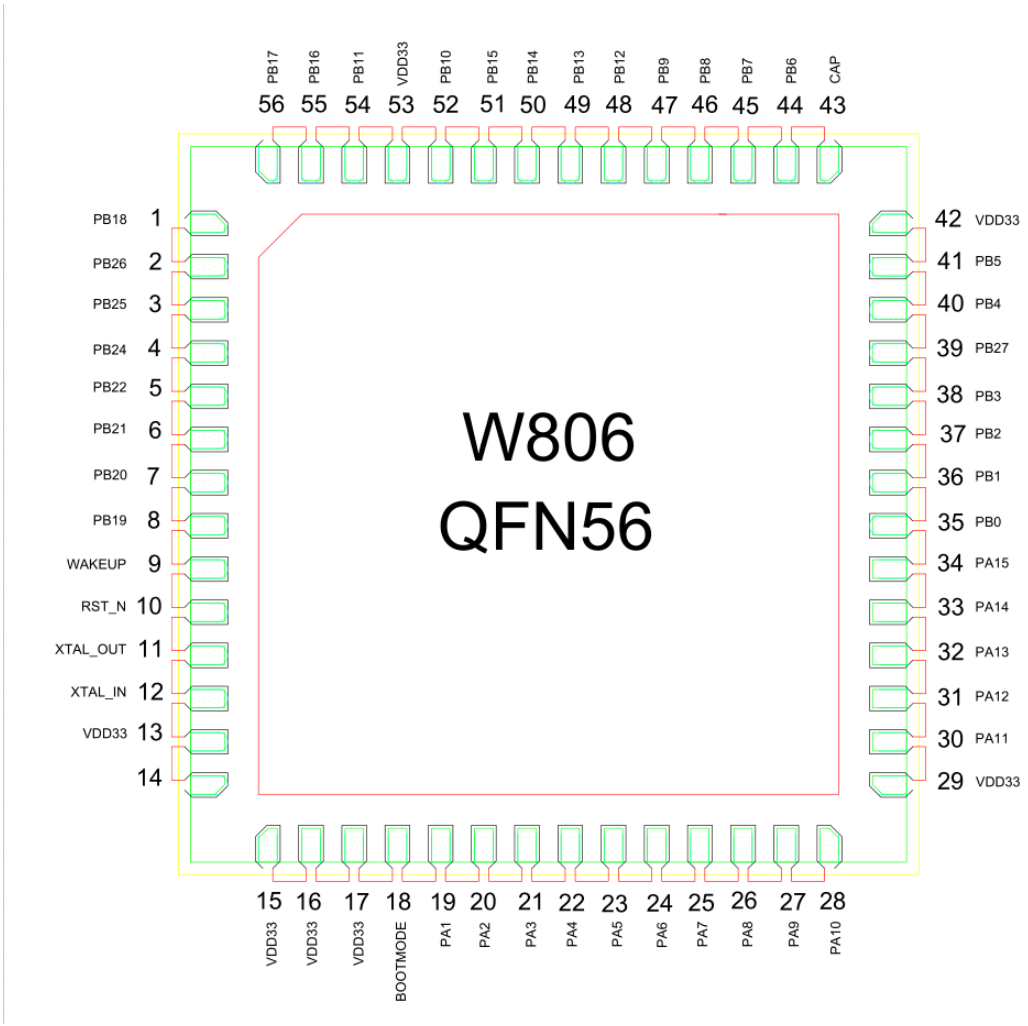


Figure 2-1 Pin layout (QFN56).

No.	Name	Type	Pin function after reset	Alt. function	Max. frequency	Pull-up and pull-down capability	max. current)
1	PB_18	I/O	GPIO, input, high impedance	UART5_TX/LCD_SEG30	10 MHz	UP/DOWN	12 mA
2	PB_26	I/O	GPIO, input, high impedance	LSPI_MOSI/PWM4/LCD_SEG1	20 MHz	UP/DOWN	12 mA
3	PB_25	I/O	GPIO, input, high impedance	LSPI_MISO/PWM3/LCD_COM0	20 MHz	UP/DOWN	12 mA
4	PB_24	I/O	GPIO, input, high impedance	LSPI_CK/PWM2/LCD_SEG2	20 MHz	UP/DOWN	12 mA
5	PB_22	I/O	GPIO, input, high impedance		10 MHz	UP/DOWN	12 mA
6	PB_21	I/O	GPIO, input, high impedance		10 MHz	UP/DOWN	12 mA
7	PB_20	I/O	UART_RX	UART0_RX/PWM1/UART1_CTS/I2C_SCL	10 MHz	UP/DOWN	12 mA
8	PB_19	I/O	UART_TX	UART0_TX/PWM0/UART1_RTS/I2C_SDA	10 MHz	UP/DOWN	12 mA
9	WAKEUP	I	WAKEUP wake-up function				
10	RESET	I					
11	XTAL_OUT	O					

12	XTAL_IN	I					
13	VDD33	P					
14	NC						
15	VDD33	P					
16	VDD33	P					
17	VDD33	P					
18	BOOTMODE	I/O	BOOTMODE	I2S_MCLK/LSPI_CS/PWM2/I2S_DO	20MHz	UP/DOWN	12mA
19	PA_1	I/O	JTAG_CK	JTAG_CK/I2C_SCL/PWM3/I2S_LRCK/ADC_1	20MHz	UP/DOWN	12mA
20	PA_2	I/O	GPIO, input, high impedance	UART1_RTS/UART2_TX/PWM0/UART3_RTS/ADC_4	20MHz	UP/DOWN	12mA
21	PA_3	I/O	GPIO, input, high impedance	UART1_CTS/UART2_RX/PWM1/UART3_CTS/ADC_3	20MHz	UP/DOWN	12mA
22	PA_4	I/O	JTAG_SWO	JTAG_SWO/I2C_SDA/PWM4/I2S_BCK/ADC_2	20MHz	UP/DOWN	12mA
23	PA_5	I/O	GPIO, input, high impedance	UART3_TX/UART2_RTS/PWM_BREAK/UART4_RTS/VRP_EXT	20MHz	UP/DOWN	12mA
24	PA_6	I/O	GPIO, input, high impedance	UART3_RX/UART2_CTS/NULL/UART4_CTS/LCD_SEG31/VRP_EXT	20MHz	UP/DOWN	12mA
25	PA_7	I/O	GPIO, input, high impedance	PWM4/LSPI_MOSI/I2S_MCK/I2S_DI/LCD_SEG3/Touch_1	20MHz	UP/DOWN	12mA
26	PA_8	I/O	GPIO, input, high impedance	PWM_BREAK/UART4_TX/UART5_TX/I2S_BCLK/LCD_SEG4	20MHz	UP/DOWN	12mA
27	PA_9	I/O	GPIO, input, high impedance	MMC_CLK/UART4_RX/UART5_RX/I2S_LRCLK/LCD_SEG5/TOUCH_2	50MHz	UP/DOWN	12mA
28	PA_10	I/O	GPIO, input, high impedance	MMC_CMD/UART4_RTS/PWM0/I2S_DO/LCD_SEG6/TOUCH_3	50MHz	UP/DOWN	12mA
29	VDD33	P	Chip power supply, 3.3V				
30	PA_11	I/O	GPIO, input, high impedance	MMC_DAT0/UART4_CTS/PWM1/I2S_DI/LCD_SEG7	50MHz	UP/DOWN	12mA
31	PA_12	I/O	GPIO, input, high impedance	MMC_DAT1/UART5_TX/PWM2/LCD_SEG8/TOUCH_14	50MHz	UP/DOWN	12mA
32	PA_13	I/O	GPIO, input, high impedance	MMC_DAT2/UART5_RX/PWM3/LCD_SEG9	50MHz	UP/DOWN	12mA
33	PA_14	I/O	GPIO, input, high impedance	MMC_DAT3/UART5_CTS/PWM4/LCD_SEG10/TOUCH_15	50MHz	UP/DOWN	12mA
34	PA_15	I/O	GPIO, input, high impedance	PSRAM_CK/UART5_RTS/PWM_BREAK/LCD_SEG11	50MHz	UP/DOWN	12mA
35	PB_0	I/O	GPIO, input, high impedance	PWM0/LSPI_MISO/UART3_TX/PSRAM_CK/LCD_SEG12/Touch_4	80MHz	UP/DOWN	12mA
36	PB_1	I/O	GPIO, input, high impedance	PWM1/LSPI_CK/UART3_RX/PSRAM_CS/LCD_SEG13/Touch_5	80MHz	UP/DOWN	12mA
37	PB_2	I/O	GPIO, input, high impedance	PWM2/LSPI_CK/UART2_TX/PSRAM_D0/LCD_SEG14/Touch_6	80MHz	UP/DOWN	12mA
38	PB_3	I/O	GPIO, input, high impedance	PWM3/LSPI_MISO/UART2_RX/PSRAM_D1/LCD_SEG15/Touch_7	80MHz	UP/DOWN	12mA
39	PB_27	I/O	GPIO, input, high impedance	PSRAM_CS/UART0_TX/LCD_COM3	80MHz	UP/DOWN	12mA
40	PB_4	I/O	GPIO, input, high impedance	LSPI_CS/UART2_RTS/UART4_TX/PSRAM_D2/LCD_SEG16/Touch_8	80MHz	UP/DOWN	12mA
41	PB_5	I/O	GPIO, input, high impedance	LSPI_MOSI/UART2_CTS/UART4_RX/PSARM_D3/LCD_SEG17/Touch_9	80MHz	UP/DOWN	12mA
42	VDD33	P	Chip power supply, 3.3V				
43	CAP	I	External capacitor, 4.7μF				
44	PB_6	I/O	GPIO, input, high impedance	UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK/LCD_SEG18/Touch_10	50MHz	UP/DOWN	12mA
45	PB_7	I/O	GPIO, input, high impedance	UART1_RX/MMC_CMD/HSPI_INT/SDIO_CMD/LCD_SEG19/Touch_11	50MHz	UP/DOWN	12mA
46	PB_8	I/O	GPIO, input, high impedance	I2S_BCK/MMC_D0/PWM_BREAK/SDIO_D0/LCD_SEG20/Touch_12	50MHz	UP/DOWN	12mA
47	PB_9	I/O	GPIO, input, high impedance	I2S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/LCD_SEG21/Touch_13	50MHz	UP/DOWN	12mA
48	PB_12	I/O	GPIO, input, high impedance	HSPI_CK/PWM0/UART5_CTS/I2S_BCLK/LCD_SEG24	50MHz	UP/DOWN	12mA
49	PB_13	I/O	GPIO, input, high impedance	HSPI_INT/PWM1/UART5_RTS/I2S_LRCLK/LCD_SEG25	50MHz		
50	PB_14	I/O	GPIO, input, high impedance	HSPI_CS/PWM2/LSPI_CS/I2S_DO/LCD_SEG26	50MHz	UP/DOWN	12mA

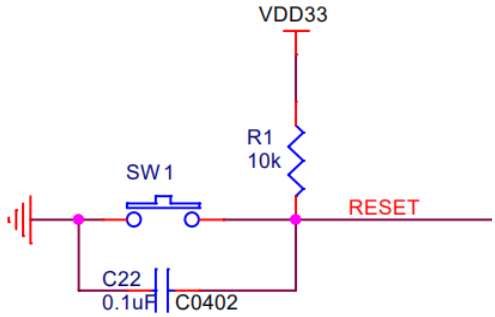
51	PB_15	I/O	GPIO, input, high impedance	HSPI_DI/PWM3/LSPI_CK/I2S_DI/LCD_SEG27	50MHz	UP/DOWN	12mA
52	PB_10	I/O	GPIO, input, high impedance	I2S_DI/MMC_D2/HSPI_DI/SDIO_D2/LCD_SEG22	50MHz	UP/DOWN	12mA
53	VDD33	P	Chip power supply, 3.3V				
54	PB_11	I/O	GPIO, input, high impedance	I2S_DO/MMC_D3/HSPI_DO/SDIO_D3/LCD_SEG23	50MHz	UP/DOWN	12mA
55	PB_16	I/O	GPIO, input, high impedance	HSPI_DO/PWM4/LSPI_MISO/UART1_RX/LCD_SEG28	50MHz	UP/DOWN	12mA
56	PB_17	I/O	GPIO, input, high impedance	UART5_RX/PWM_BREAK/LSPI_MOSI/I2S_MCLK/LCD_SEG29	20MHz	UP/DOWN	12mA
57	GND	P	Chip Bottom Ground PAD				

Notes: 1. I = Input, O = Output, P = Power

3 Chip Peripheral Circuit Design.

3.1 RESET circuit design

The reset circuit is recommended to be designed as an RC circuit, which automatically resets when powered on, and resets at a low level of W806. If using an external control RESET pipe pin, when the level value is lower than 2.0v, the chip is in reset state. The low level must last for more than 100us during reset, see Figure 3-1.



The Figure 3-1 Reset circuit

3.2 Reference Clock Circuit Design

The chip reference clock uses a frequency of 40MHz, and customers can choose different temperature levels, stability, and load capacitance values according to actual product requirements of crystals.

load capacitance connected to both ends of the crystal needs to be adjusted according to the crystal of different manufacturers and the frequency offset. See Figure 3-2 in the reference design.

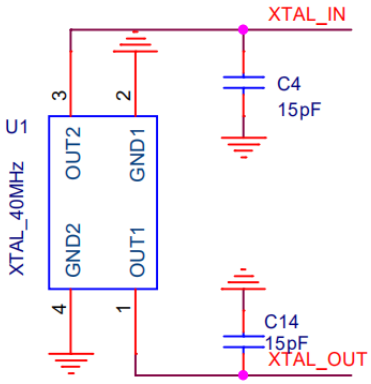


Figure 3-2 Crystal circuit

The crystal should be placed as close to the chip as possible, the traces should be as short as possible, and away from interference sources, and there are multiple ground holes around the clock for isolation. The layers below the clock disable its It is routed through to prevent interference with the clock source.

3.3 ADC circuit design.

The 19~21 pins of the chip can be used as ordinary ADC, and the input voltage range is 0~2.4V. When it is higher than 2.4V, the external voltage divider needs to be processed before access to ADC interface. To improve accuracy, use high precision resistors for R1 and R2. Select appropriate R1, R2 according to Sensor output voltage value resistor value divider. As shown in Figure 3-3

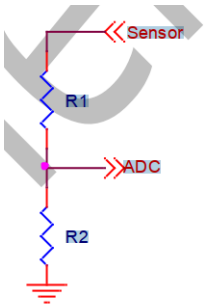


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Figure 3-3 ADC voltage divider circuit

3.4 WAKEUP circuit design

After the chip enters the sleep state, the WAKEUP function can be used to wake up the chip, and the WAKEUP pin input high level can wake up chip from the sleep state.

When the chip is in normal working state, the WAKEUP pin is low and can pull down the 10K resistor.

Note that if the WAKEUP function is not used, this pin can be left floating or pulled down, but cannot be pulled up.

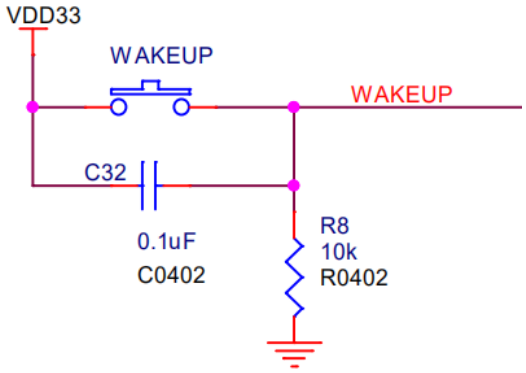


Figure 3-4 WAKEUP circuit

3.5 GPIO Design

After the chip is powered on, pins 7 and 8 are UART0 ports by default, which provide download and AT command ports and log output ports. customer use

Be careful not to use this port as GPIO at will, to prevent it from being occupied and unable to download and debug. After the system is up, the port can be reset

used for other ports. If the port is occupied, you can operate according to chapter 3.7.

Table 3-2 Chip UART0 pin description

7	PB20	I/O	UART0_RX
8	PB19	I/O	UART0_TX

The multiplexing relationship and usage of other pins are shown in Table 2-1. All GPIO if the chip is internally configured as pull-up, the typical pull-up resistor value is 40K, if configured as pull-down, the typical pull-down resistor value is 49K.

3.6 Touch Sensor Design.

W806 integrates 15 Touch Sensors inside. See Table 2-1 for detailed pin definitions. When designing, attention should be paid to the parasitics of traces and external circuits.

The influence of capacitance, the size of parasitic capacitance directly affects the sensitivity of Touch Sensor.

Figure 3-6 is a schematic diagram of the touch capacitance distribution, where Cground is the capacitance between the reference ground of the touch circuit and the ground, and Ccomponent is the parasitic capacitance inside the chip, parasitic capacitance between Ctrace trace and circuit reference ground, between Celectrode touch electrode and circuit reference ground. The parasitic capacitance of Ctouch, the capacitance formed by the Ctouch finger and the touch electrode relative to the ground.

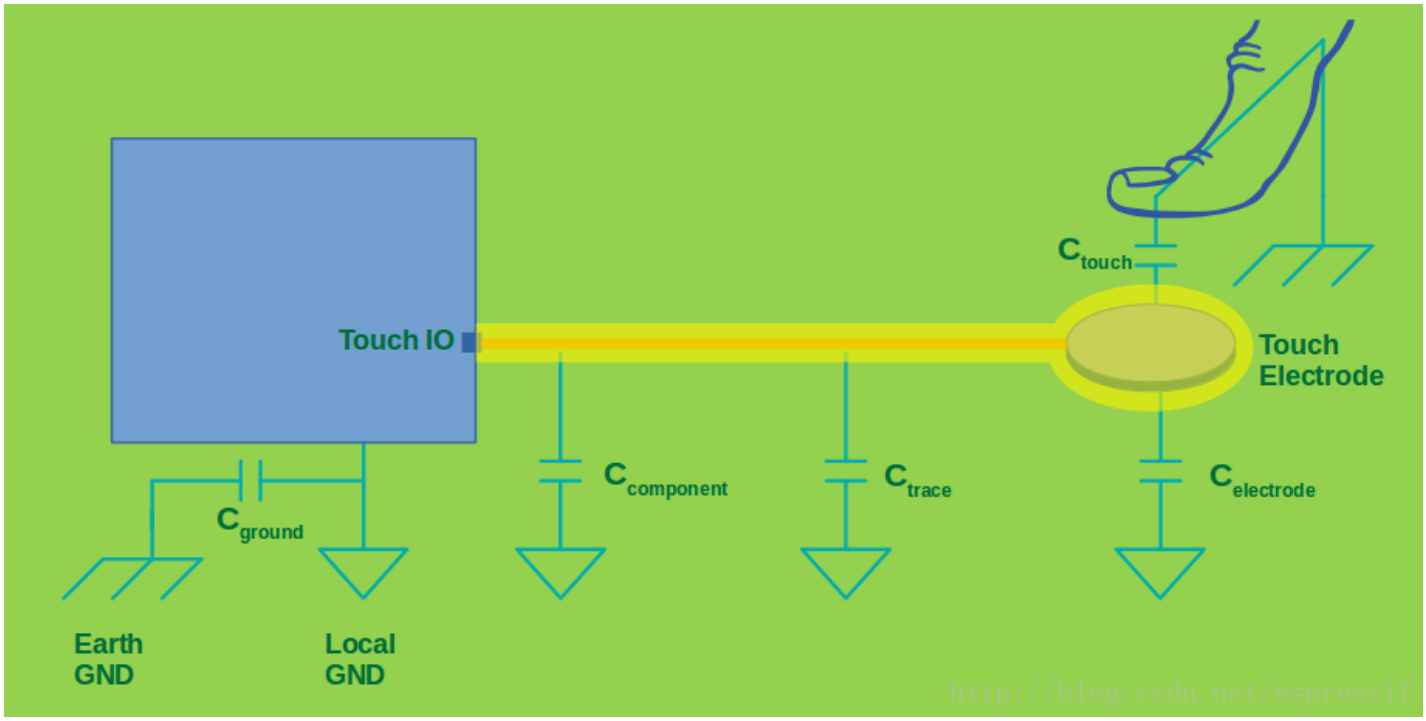


Figure 3-6 Schematic diagram of touch capacitance distribution

Parasitic capacitance Cp (that is, the capacitance when no touch action occurs)=Ccomponent+Ctrace+Celectrode. When a touch action occurs, the change of the total capacitance of the system ΔC=Ctouch, the common Ctouch is about 5pF~15pF. When the parasitic capacitance Cp is smaller and Ctouch is larger, the easier the touch action is to be detected by the system, the higher the sensitivity of the touch sensing system. When using this part of the function, you need to refer to related content of the "touch_sensor Software and Hardware Design Guide v1.0" document.

3.7 Download port.

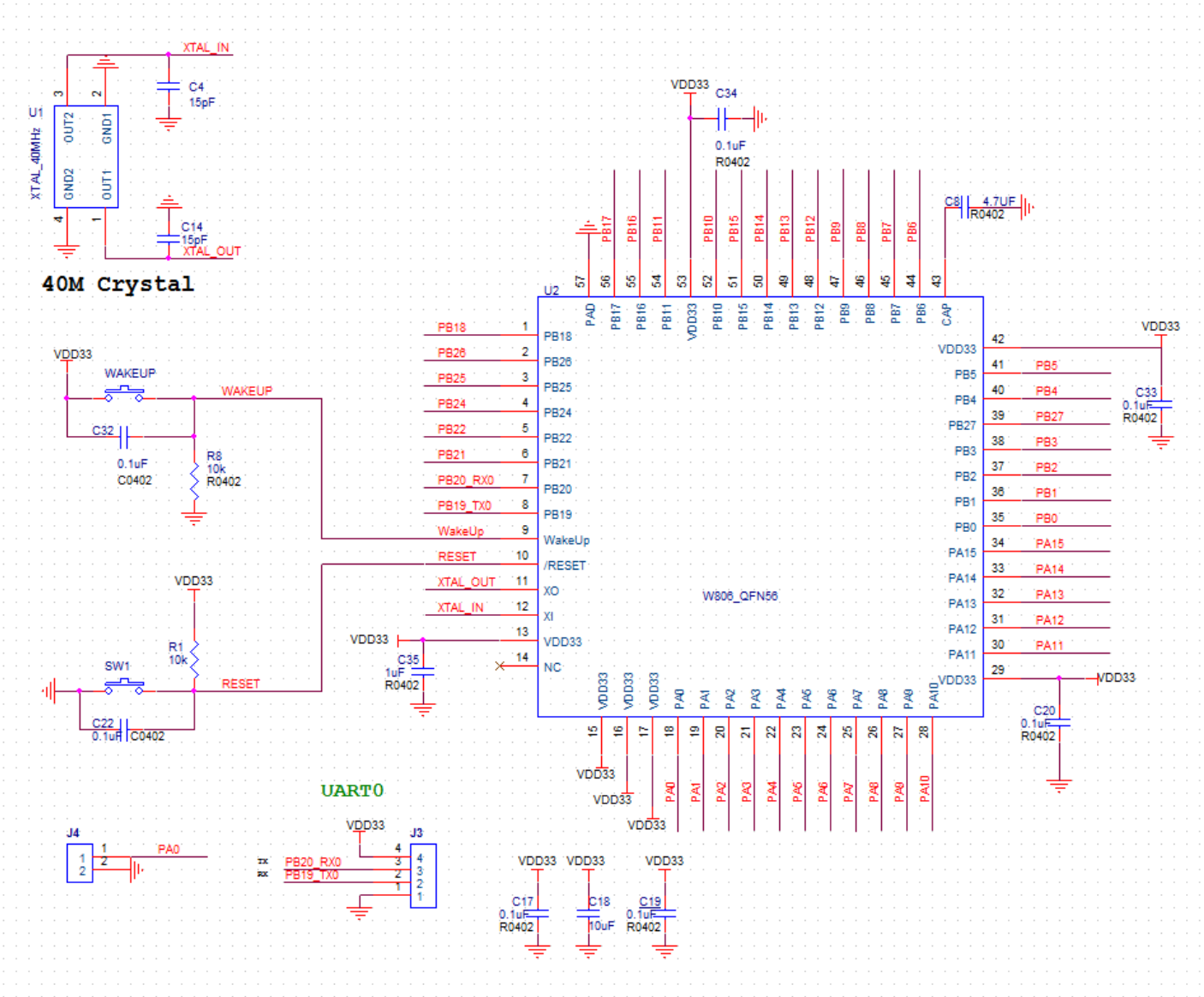
The W806 chip defaults to UART0 as the download port. When the chip has no firmware for initial download, it can directly connect to the UART0 interface and use the relevant download software firmware can be downloaded. When there is firmware in the chip, enter the download mode again, you can pull down BOOTMODE, and then power on to enter the down load mode. After the download is complete, remove the operation of lowering BOOTMODE, and it needs to be restarted before the firmware can run.

3.8 Power Design.

Chip power supply voltage: 3.3V, normal working power supply range: 3.0V-3.6V. Do not exceed this range, over 3.6V may cause permanent damage to the chip

lower than 3.0V may degrade the overall performance, the total current is recommended to be more than 500mA. Each power input pin of the chip should be placed accordingly filter capacitor.

3.9 Reference Design Schematic.



4 Layout design

The PAD in the middle of the W806 chip is the heat dissipation ground pad, which needs to be grounded. At the same time, it needs to be punched to make good contact with the ground for heat dissipation. The middle belly do not use window design for vias. Figure 4-1.

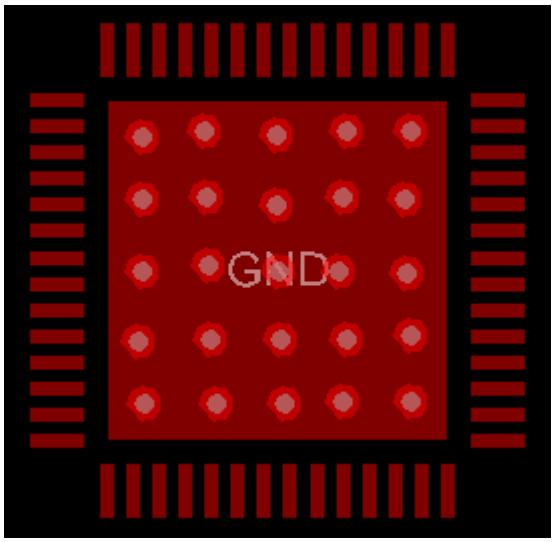


Figure 4-1 Ground Pad Handling